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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,395	08/14/2008	Hien Boon Tan	Q78657	3868

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EXAMINER	
GOODWIN, DAVID J	

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,395	TAN ET AL.	
	Examiner	Art Unit	
	DAVID GOODWIN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *10-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/28/7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities:

2. Claim 1 recites “attaching an array of two or more integrated circuit chips on a substrate. This suggests that the plurality of chips are attached “to" each other rather than “to" the substrate.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Chakravorty (US 6181569).

3. Regarding claim 1.

4. Chakravorty teaches a method of making a device. Said method comprises providing a chip array (317) each array comprising two or more integrated circuit chips (fig 9a). Attaching each chip array (317) to a substrate (318) (fig 9b) (column 12 lines 35-55). Dicing each array (317), attached to the substrate(318) into individual chip scale packages, each individual chip scale package (314) comprising only one integrated circuit chip (fig 9e) (column 13 lines 5-25).

5. Regarding claim 3.

6. Chakravorty teaches a method of making a device. Said method comprises providing a wafer, the wafer comprising a plurality of integrated circuit chips, and dicing the wafer into a plurality of chip arrays (317) each array comprising two or more integrated circuit chips (fig 9a). Attaching each chip array (317) to a substrate (318) (fig 9b) (column 12 lines 35-55). Dicing each array (317), attached to the substrate(318) into individual chip scale packages, each individual chip scale package (314) comprising only one integrated circuit chip (fig 9e) (column 13 lines 5-25).

7. Regarding claim 4.

8. Each array comprises a 2X2 matrix (fig 9e).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) as applied to claim 1 and further in view of Qi (US 6774497).

11. Regarding claim 2.

12. Chakrovorty teaches elements of the claimed invention above.

13. Chakrovorty does not teach bond pads on the chip.

14. Qi teaches forming a chip (110) having a plurality of bond pads (114) in a single row and centrally disposed on an upper surface of the integrated circuit chip (110). A

plurality of conductive bumps (120) formed on the plurality of bond pads (114) (fig 1) (column 4 lines 45-65).

15. It would have been obvious to one of ordinary skill in the art to form a chip having bond pads so that conductive traces can be connected to the chip.

16. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497).

17. Regarding claim 5.

18. Chakravorty teaches a method of making a device. Said method comprises providing a wafer, the wafer comprising a plurality of integrated circuit chips, and dicing the wafer into a plurality of chip arrays (317) each array comprising two or more integrated circuit chips (fig 9a). Attaching each chip array (317) to a substrate (318) (fig 9b) (column 12 lines 35-55). Dicing each array (317), attached to the substrate(318) into individual chip scale packages, each individual chip scale package (314) comprising only one integrated circuit chip (fig 9e) (column 13 lines 5-25).

19. Chakravortry does not teach the mounting process.

20. Qi teaches a method of making a device. Said method comprises a chip (110) having a plurality of bond pads (114) aligned on an upper surface of the integrated circuit chip. A plurality of conductive bumps (120) formed on the plurality of bond pads (114) (fig 1) (column 4 lines 45-65). Mounting each chip on a substrate (240) such that the bumps align with corresponding solder pad openings (242) on an upper surface of the substrate (240) (fig 2a). Reflowing the chips thereby melting the bumps and establishing a conductive joint between the integrated circuit chips and the substrate (fig

2b). Under fill encapsulating the integrated circuit chip on the substrate (fig 2b) (column 6 lines 1-45).

21. It would have been obvious to one of ordinary skill in the art to form a chip having bond pads so that conductive traces can be connected to the chip.

22. Regarding claim 6.

23. Qi teaches, prior to mounting, dipping each array in flux material such that flux (124) material adheres to the bumps (120) (fig 1). Wherein each array is mounted on a substrate the flux material adheres the bumps to the solder pad openings (242) (fig 2a) (column 5 lines 20-25).

24. Claim 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497) and further in view of Lance (US 5697148)

25. Regarding claim 7

26. Chakravorty in view of Qi teaches elements of the claimed invention above.

27. Chakravorty in view of Qi does not teach cleaning the flux from the device

28. Lance teaches cleaning the flux from the device (column 1 lines 20-35).

29. It would have been obvious to on e of ordinary skill in the art to clean the fluc from the device in order to prevent corrosion.

30. Regarding claim 8

31. Chakravorty in view of Qi teaches elements of the claimed invention above.

32. Chakravorty in view of Qi does not teach injecting the encapsulant.

33. Lance teaches injecting the encapsulant (22) between the chip (12) and the substrate (14).

34. It would have been obvious to one of ordinary skill in the art to inject the encapsulant in order to alleviate problems of thermal mismatch.

35. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497) and further in view of Ho (US 6849955)

36. Regarding claim 9.

37. Chakravorty in view of Qi teaches elements of the claimed invention above.

38. Chakravorty in view of Qi does not teach solder balls formed on the backside of the substrate.

39. Ho teaches forming solder balls (510)formed on the back side of the carrier substrate (100) (fig 8).

40. It would have been obvious to one of ordinary skill in the art to form solder balls on the back side of the carrier substrate in order for the substrate to be electrically connected to a circuit board.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID GOODWIN whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

djg

/STEVEN LOKE/

Supervisory Patent Examiner, Art Unit 2818